ABSTRACT OF THE DISCLOSURE

An arbiter performs activation of memory that corresponds to a bus access request from DSP in parallel with an access to memory that corresponds to a bus access request from CPU, when DSP requests to access the bus before the access to memory that corresponds to the bus access request from CPU has been completed. Therefore, immediately after the access to memory that corresponds to the bus access request from CPU has been completed, the access to memory that corresponds to the bus access request from DSP is allowed, thereby improving processing performance.